## TOSHIBA

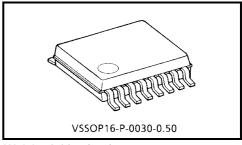
Preliminary TOSHIBA CMOS Digital Integrated Circuit Sillicon Monolithic

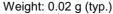
# TC7MZ4051FK, TC7MZ4052FK, TC7MZ4053FK

TC7MZ4051FK 8-Channel Analog Multiplexer/Demultiplexer TC7MZ4052FK Dual 4-Channel Analog Multiplexer/Demultiplexer TC7MZ4053FK Triple 2-Channel Analog Multiplexer/Demultiplexer

The TC7MZ4051/4052/4053FK are high-speed, low-voltage drive analog multiplexer/demultiplexers using silicon gate CMOS technology. In 3 V and 5 V systems these can achieve high-speed operation with the low power dissipation that is a feature of CMOS.

The TC7MZ4051/4052/4053FK offer analog/digital signal selection as well as mixed signals. The 4051 has an 8-channel configuration, the 4052 has an 4-channel  $\times$  2 configuration, and the 4053 has a 2-channel  $\times$  3 configuration.





The switches for each channel are turned ON by the control pin digital signals.

Although the control signal logical amplitude ( $V_{CC}$  – GND) is small, the device can perform large-amplitude ( $V_{CC}$  –  $V_{EE}$ ) signal switching.

For example, if  $V_{CC} = 3 V$ , GND = 0 V, and  $V_{EE} = -3 V$ , signals between -3 V and +3 V can be switched from the logical circuit using a single 3 V power supply.

All input pins are equipped with a newly developed input protection circuit that avoids the need for a diode on the plus side (forward side from the input to the  $V_{CC}$ ). As a result, for example, 5 V signals can be permitted on the inputs even when the power supply voltage to the circuits is off. As a result of this input power protection, the TC7MZ4051/4052/4053FK can be used in a variety of applications, including in the system which has two power supplies, and in battery backup circuits.

### Features

• Low ON resistance:  $R_{on} = 65 \Omega$  (typ.) (V<sub>CC</sub> - V<sub>EE</sub> = 3 V)  $R_{on} = 45 \Omega$  (typ.) (V<sub>CC</sub> - V<sub>EE</sub> = 6 V)

- High speed:  $t_{pd} = 5 \text{ ns} (typ.) (V_{CC} = 3.0 \text{ V})$
- Low power dissipation:  $I_{CC} = 4 \mu A (max) (T_a = 25^{\circ}C)$
- Input level:  $V_{IL} = 0.8 V (max) (V_{CC} = 3 V)$  $V_{IH} = 2.0 V (min) (V_{CC} = 3 V)$
- Power down protection is provided on all control inputs
- Pin and function compatible with 74HC4051/4052/4053

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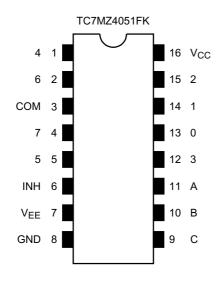
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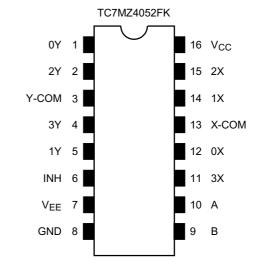
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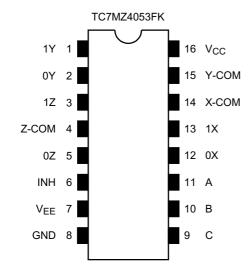
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## Pin Assignment (top view)







## **Truth Table**

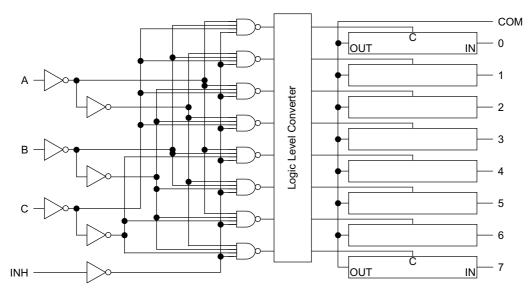
	Contro	l Inputs		"ON" Channel				
Inhibit	C*	В	А	MZ4051	MZ4052	MZ4053		
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z		
L	L	L	Н	1	1X, 1Y	1X, 0Y, 0Z		
L	L	Н	L	2	2X, 2Y	0X, 1Y, 0Z		
L	L	Н	Н	3	3X, 3Y	1X, 1Y, 0Z		
L	н	L	L	4	_	0X, 0Y, 1Z		
L	н	L	Н	5	_	1X, 0Y, 1Z		
L	н	Н	L	6		0X, 1Y, 1Z		
L	н	Н	Н	7	_	1X, 1Y, 1Z		
Н	Х	Х	Х	None	None	None		

X: Don't care, \*: Except MZ4052

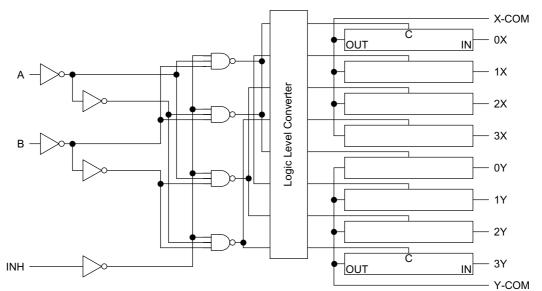
## **TOSHIBA**

## System Diagram

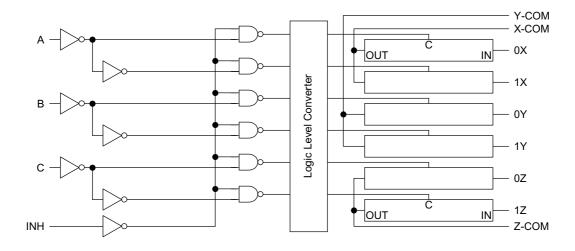
### TC7MZ4051FK



### TC7MZ4052FK



### TC7MZ4053FK



## Absolute Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V <sub>CC</sub>	-0.5~7.0	V
Tower supply voltage	V <sub>CC</sub> ~V <sub>EE</sub>	-0.5~7.0	v
Control input voltage	V <sub>IN</sub>	-0.5~7.0	V
Switch I/O voltage	V <sub>I/O</sub>	$V_{EE} - 0.5 \text{-} V_{CC} + 0.5$	V
Input diode current	IIK	-20	mA
I/O diode current	liok	±20	mA
Switch through current	Ι <sub>Τ</sub>	±25	mA
DC $V_{CC}$ or ground current	ICC	±50	mA
Power dissipation	PD	180	mW
Storage temperature	T <sub>stg</sub>	-65~150	°C

## **Recommended Operating Conditions**

Characteristics	Symbol	Rating	Unit	
	V <sub>CC</sub>	2~6		
Power supply voltage	VEE	-4~0	V	
	V <sub>CC</sub> ~V <sub>EE</sub>	2~6	l	
Input voltage	V <sub>IN</sub>	0~6.0	V	
Switch I/O voltage	V <sub>I/O</sub>	V <sub>EE</sub> ~V <sub>CC</sub>	V	
Operating temperature	T <sub>opr</sub>	-40~85	°C	
Input rise and fall time	dt/dv	0~100	ns/V	

## **Electrical Characteristics**

### **DC Electrical Characteristics**

Characteristics		Symbol Test Condition		_		-	Ta = 25°C			Ta = -40~85°C		
		Symbol	Test Condition	$V_{EE}(V)$	$V_{CC}(V)$	Min	Тур.	Max	Min	Max	Unit	
					2.0	1.5		_	1.5	_		
	High-level	VIH	—		3.0	2.0	_	_	2.0	_		
Input voltage					6.0	4.2	—		4.2	_	V	
input voitage					2.0		_	0.5		0.5	v	
	Low-level	VIL	—		3.0	_		0.8		0.8		
				-	6.0		_	1.8		1.8		
			$V_{IN} = V_{IL} \text{ or } V_{IH}$	GND	3.0	_	_	150		180		
	ON resistance		$V_{I/O} = V_{CC}$ to $V_{EE}$ $I_{I/O} = 2 \text{ mA}$	-3.0	3.0	—	—	100	—	125	0	
ON resistance			$V_{IN} = V_{IL} \text{ or } V_{IH}$	GND	2.0			_		—	Ω	
			$V_{I/O} = V_{CC} \text{ or } V_{EE}$	GND	3.0	_	50	120	_	150		
			$I_{I/O} = 2 \text{ mA}$	-3.0	3.0		30	80		100	100	
Difference of O	N	∆R <sub>ON</sub>	$V_{IN} = V_{IL} \text{ or } V_{IH}$	GND	2.0		10	_				
resistance betw			$V_{I/O} = V_{CC}$ to $V_{EE}$	GND	3.0	_	5	15		20	Ω	
switches			$I_{I/O} = 2 \text{ mA}$	-3.0	3.0		5	10		15		
Input/Output lea	akaqe	V <sub>OS</sub> = V <sub>CC</sub> or		GND	3.0		_	±0.25		±2.5		
current (switch OFF)		_	$V_{IS} = GND \text{ to } V_{CC}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$	-3.0	3.0	—	_	±0.5	_	5.0	μA	
Input/Output leakage current (switch ON, output open)		$V_{OS} = V_{CC}$ or GN	$V_{OS} = V_{CC} \text{ or } GND$	GND	3.0	_	_	±0.25		±2.5		
		I <sub>IN</sub>	$V_{IN} = V_{IL} \text{ or } V_{IH}$	-3.0	3.0	_		±0.5		±5.0	μA	
Control input cu	irrent	I <sub>IN</sub>	$V_{IN} = V_{CC}$ or GND	GND	6.0	_	_	±0.1	_	±0.1	μA	
Quiescent supp	ly current	loo	V <sub>IN</sub> = V <sub>CC</sub> or GND	GND	3.0	_		4.0		40.0	μA	
Quiescent supp	iy current	Icc		-3.0	3.0			8.0		80.0	μΑ	

## AC Electrical Characteristics (CL = 50 pF, Input: $t_r = t_f = 3 \text{ ns}$ , GND = 0 V)

Observation	Quarter	T				-	Ta = 25°C			Ta = -40~85°C	
Characteristics	Symbol	les	Test Condition		$V_{CC}(V)$	Min	Тур.	Max	Min	Max	Unit
Phase difference between					2.0	_	10		_		- ns
	11/0	All types		GND	3.0		5		_		
input and output	φl/O			GND	4.5	_	4		_		
				-3.0	3.0		3				
				GND	2.0				_		
			Figure 1, Figure 5	GND	3.0	_	8		_		
		4051	(Note1)	GND	4.5	_			_		
			(	-3.0	3.0	_			_		
				GND	2.0				_		
O de de malde l'an	t <sub>pZL</sub>	1050	Figure 1, Figure 5	GND	3.0		8		_		
Output enable time	t <sub>pZH</sub>	4052	(Note1)	GND	4.5	_			_		ns
			(	-3.0	3.0	_			_		
			Figure 1, Figure 5 (Note1)	GND	2.0				_		
		4050		GND	3.0		6		_		
		4053		GND	4.5				_		
			(110101)	-3.0	3.0					_	
	t <sub>pLZ</sub>	4051	Figure 1, Figure 5 (Note1)	GND	2.0				_		- ns
				GND	3.0		10		_		
				GND	4.5				_		
				-3.0	3.0				_		
			Figure 1, Figure 5 (Note1)	GND	2.0	_			_		
				GND	3.0	_	10		_		
Output disable time	t <sub>pHZ</sub>	4052		GND	4.5	_			_		
				-3.0	3.0	_			_		
				GND	2.0	_			_		
		1050	Figure 1, Figure 5	GND	3.0	_	9		_		
		4053	(Note1)	GND	4.5				—		
			(	-3.0	3.0				_		
Control input capacitance	C <sub>in</sub>	All type	es (Note2)	_	_	_					pF
COMMON terminal capacitance	C <sub>IS</sub>	4051 4052 4053	Figure 2 (Note2)	-3.0	3.0		TBD		_	_	pF
SWITCH terminal capacitance	C <sub>OS</sub>	4051 4052 4053	Figure 2 (Note2)	-3.0	3.0		TBD		_	_	pF
Feedthrough capacitance	C <sub>IOS</sub>	4051 4052) 4053	Figure 2 (Note2)	-3.0	3.0		TBD				pF
Power dissipation capacitance	C <sub>PD</sub>	4051 4052 4053	Figure 2 (Note2)	GND	6.0	_	TBD	_	_	_	pF

Note1:  $R_L = 500 \Omega$ 

Note2:  $C_{in}$ ,  $C_{I}$ ,  $C_{OS}$  and  $C_{IOS}$  are guaranteed by the design.

Note3: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current can be obtained by the equiation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$ 

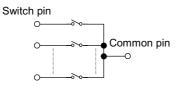
## Analog Switch Characteristics (GND = 0 V, Ta = 25°C)

Characteristics	Symbol	Test Condition			r	Тур.	Unit
Characteriotice	Cymbol	root contaiton	$V_{EE}\left(V\right)$	$V_{CC}(V)$	199.	Onit	
		Adjust V <sub>IN</sub> so that the output is 0 All (Noted dBm. Now measure the frequency					
Frequency response (switch ON)	f <sub>max</sub>	when the output drops $-3$ dB. R <sub>L</sub> = 50 $\Omega$ , C <sub>L</sub> = 10 pF, f <sub>IN</sub> = 1 MHz, sine wave	4051 4052 (Note5) 4053	-3.0	3.0		MHz
Crosstalk (between any switches)		Figure 3 Measure the leak voltage when V <sub>IN</sub> is adjusted so that the input is 0 dBm. $R_L = 600 \Omega$ , $C_L = 50 pF$ , $f_{IN} = 1 MHz$ , sine wave Figure 4		-3.0	3.0	-50	dB

Note4: Input COMMON terminal, and measured at SWITCH terminal.

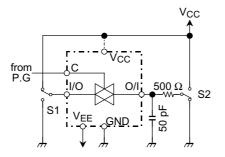
Note5: Input SWITCH terminal, and measured at COMMON terminal.

\*: These characterictics are determined by design of devices.

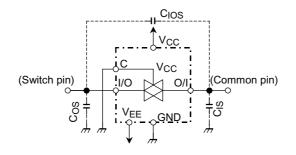


# <u>TOSHIBA</u>

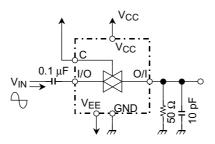
## **AC Test Circuit**



 $\label{eq:Figure 1} \begin{array}{c} t_{pLZ},\,t_{pHZ},\,t_{pZL},\,t_{pZH} \end{array}$ 









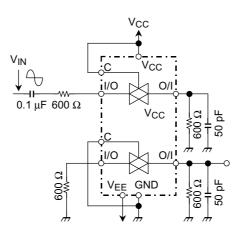
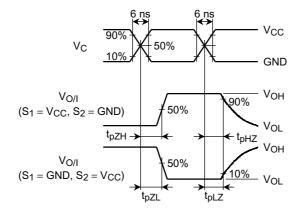
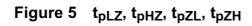


Figure 4 Cross Talk (between any two switches)

## <u>TOSHIBA</u>

## **AC Waveform**

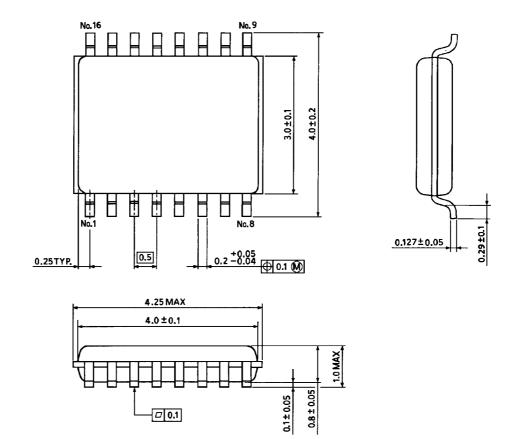




## **Package Dimensions**

VSSOP16-P-0030-0.50

Unit : mm



Weight: 0.02 g (typ.)